MCS-012

MCA (Revised)

Term-End Examination
June, 2009

07060

MCS-012 : COMPUTER ORGANISATION & ASSEMBLY LANGUAGE PROGRAMMING

Time : 3 hours *Maximum Marks : 100*

(Weightage 75%)

Note : *Question number **1** is compulsory and carries **40** marks. Attempt any **three** questions from the rest.*

1. (a) Add the following numbers using signed 2^s complement representation for 8 bit numbers. Indicate overflow if any **5**

(i) + 76 & - 59 (ii) + 76 & + 52

(iii) - 76 & - 52 (iv) + 52 & - 59

(b) Explain the working of a latch with the help of a diagram. How do you convert a latch to S-R flip flop. **5**

(c) A computer system has a 8k word cache organized in two way set associative manner having one cache word equal to 32 bits. Assume the main memory to be byte organized. What is the numbers of bits in the index and tag fields of the cache. **5**

(d) The seek time of a disk is 60ms .It rotates at the rate of 12000 rpm. Each track has 300 sectors. Calculate the access time of the disk. 5

(e) Let register R1=11000011 and register R2=00110011 Perform the following operations on R1 using R2. 5

(i) Selective set

(ii) Selective clear

(iii) Selective complement

(iv) Mask

(v) Clear R1 without using R2

(f) Explain the following 8086 microprocessor instructions with the help of on example each. 5

(i) DIV (ii) SHR

(iii) ROL (iv) DAA

(v) NEG

(g) Write a program in 8086 assembly language to add two single digit ASCLL numbers. You may assume that these two numbers are available in the data segment. The result should be left in AL register. 5

(h) List the differences between hardwired Control Unit and micro programmed Control Unit. 5

2. (a) Write an 8086 assembly language program for adding an array of five binary numbers. 5

(b) Design a three bit synchronous counter. Draw the necessary truth table & K maps for the same. 10

(c) Simplify the Boolean function $F=\left\{\overline{(\overline{A}+\overline{B})}+\overline{(A+\overline{B})}\right\}$ Draw the logic diagram of resultant function. 5

3. (a) Simplify the following function in SOP and POS forms by means of K.Maps. Also draw the logic diagram. 10

$F(A,B,C,D) = \sum (0, 2, 8, 9, 9, 10, 11, 14, 15)$.

(b) Define Decoders and Encoders. Draw a 3 X 8 Decoder with its truth table. 5

(c) Explain the Fetch cycle of instruction execution with the help of its micro-operations. 5

4. (a) Explain any five differences between RISC and CISC machines. 5

(b) Explain the process of interrupt handling using stack with the help of suitable diagrams. 8

(c) Explain the use of large register file in RISC processors with the help of a suitable diagrams can this large register file be substituted by cache memory justify your answer. 7

5. (a) A computer supports a virtual memory address space of IG Words, but a physical memory size of 64M words. How many bits are needed to specify an instruction address for this machine. 5

(b) Assume a computer having 64 word RAM (Assume 1 word = 16 bits) and cache memory of 8 blocks (block size=32 bits). Where we can find main memory locations (A) 10 & (B) 21 in cache if : 8

(I) Associative mapping.

(II) Direct mapping is used.

(c) Define the following and mention their use : 7

(i) FAT

(ii) SCSI

(iii) Resolution of computer screen

(iv) Flag register in 8086 processor

(v) Segment directive for 8086 processor

(vi) EXE programs

(vii) Instruction Register

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